TPL5111 Nano-Power System Timer for Power Gating

1 Features

- Selectable Time Intervals: 100 ms to 7200 s
- Timer Accuracy: 1% (typical)
- Current Consumption at 2.5 V: 35 nA (typical)
- Resistor Selectable Time Interval
- Manual Power-On Input
- One-Shot Feature
- Supply Voltage Range: 1.8 V to 5.5 V

2 Applications

- Duty Cycle Control of Battery-Powered Systems
- Internet of Things (IoT)
- Intruder Detection
- Tamper Detection
- Home Automation Sensors
- Thermostats
- Consumer Electronics
- Remote Sensor
- White Goods

3 Description

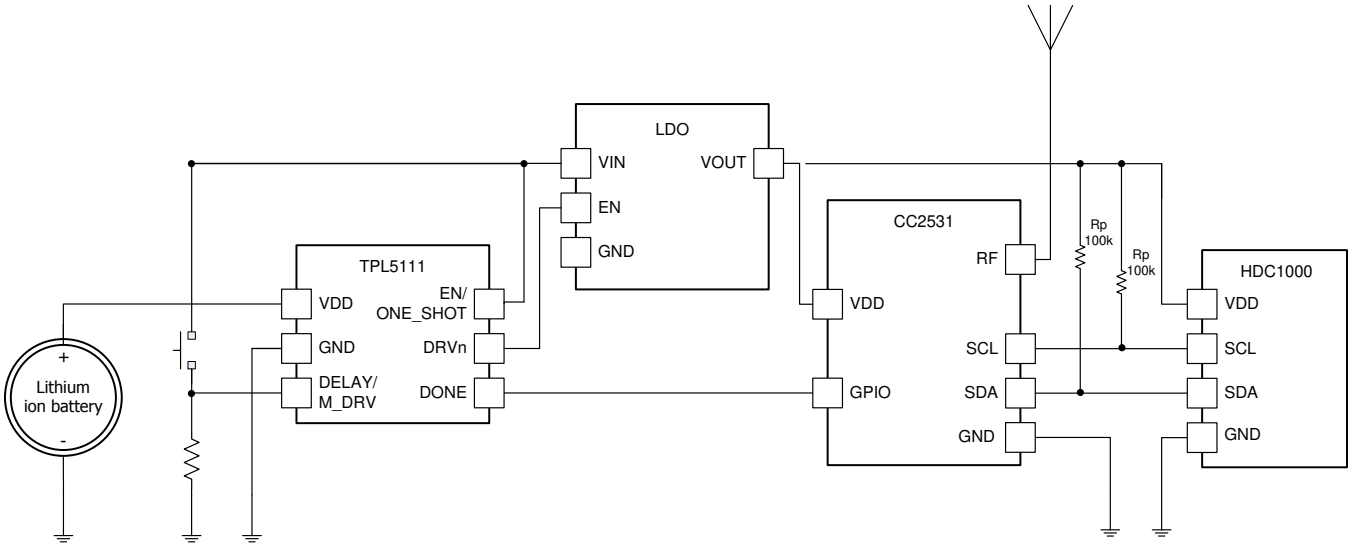
The TPL5111 Nano Timer is a low power system timer, ideal for power gating in duty cycled or battery powered applications. Consuming only 35 nA, the TPL5111 can be used to enable and disable the power supply for a micro-controller or other system device, drastically reducing the overall system stand-by current during the sleep time. This power saving enables the use of significantly smaller batteries and makes the TPL5111 well suited for energy harvesting or wireless sensor applications. The TPL5111 provides selectable timing intervals from 100 ms to 7200 s. In addition, the TPL5111 has a unique One-shot feature where the timer will only assert its enable pulse for one cycle. The TPL5111 is available in a 6 - pin SOT23 package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPL5111	SOT (6) DDC	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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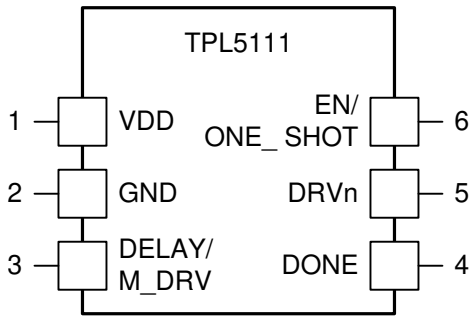
4 Revision History

Changes from Original (June 2015) to Revision A	Page
• Added full data sheet.	1

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5 Pin Configuration and Functions

DDC Package
6-Lead SOT-23
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	VDD	P	Supply voltage	
2	GND	G	Ground	
3	DELAY/ M_DRV	I	Time interval configuration (during power on) and logic input for manual Power ON	Resistance between this pin and GND is used to select the time interval. The manual Power ON signal (logic HIGH) can also connected to this pin.
4	DONE	I	Logic Input for watchdog functionality	Digital signal driven by the µC to indicate successful processing.
5	DRVn	O	Power Gating output signal generated every t_{IP}	The ENABLE pin of the LDO or DC-DC converter is connected to this pin. DRVn is active HIGH.
6	EN/ ONE_SHOT	I	Select mode of operation	When EN/ONE_SHOT = HIGH, the TPL5111 works as a TIMER. When EN/ONE_SHOT = LOW, the TPL5111 asserts DRVn one time for the programmed time interval. In this mode, the DRVn signal may be manually asserted by applying a logic HIGH to the DELAY/M_DRV pin.

(1) G= Ground, P= Power, O= Output, I= Input.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	-0.3	6.0	V
Input Voltage at any pin(2)	-0.3	VDD + 0.3	V
Input Current on any pin	-5	5	mA
Storage Temperature, T_{stg}	-65	150	°C
Junction Temperature, T_J(3)		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage between any two pins should not exceed 6V.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is PDMAX = ($T_{J(MAX)}$ - T_A)/ $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model, per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	1.8	5.5	V
Temperature	-40	105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPL5111 SOT23 DDC 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	
$R_{\theta JB}$	Junction-to-board thermal resistance	57	
ψ_{JT}	Junction-to-top characterization parameter	7.5	
ψ_{JB}	Junction-to-board characterization parameter	57	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics(1)

Specifications are for T_A= 25°C, VDD-GND=2.5 V, unless otherwise stated.

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY							
IDD	Supply current(4)	Operation mode			35	50	nA
		Digital conversion of external resistance (Rext)			200	400	µA
TIMER							
t_{IP}	Time interval Period	1650 selectable Time intervals	Min time interval		100		ms
			Max time interval		7200		s
	Time interval Setting Accuracy(5)	Excluding the precision of Rext			±0.6%		
	Time interval Setting Accuracy over supply voltage	1.8V ≤ VDD ≤ 5.5V			±25		ppm/V
t_{OSC}	Oscillator Accuracy			-0.5%		0.5%	
	Oscillator Accuracy over temperature(6)	-40°C ≤ T_A≤ 105°C			±100	±400	ppm/°C
	Oscillator Accuracy over supply voltage	1.8V ≤ VDD ≤ 5.5V			±0.4		%/V
	Oscillator Accuracy over life time(7)				±0.24%		
t_{DONE}	DONE Pulse width (6)			100			ns
t_{DRVn}	DRVn Pulse width	DONE signal not received			t_{IP}-50 ms		
t_Rext	Time to convert Rext				100	120	ms
DIGITAL LOGIC LEVELS							
VIH	Logic High Threshold DONE pin			0.7xVDD			V
VIL	Logic Low Threshold DONE pin					0.3xVDD	V
VOH	Logic output High Level DRVn pin	I_{out} = 100 µA		VDD-0.3			V
		I_{out} = 1 mA		VDD-0.7			V
VOL	Logic output Low Level DRVn pin	I_{out} = -100 µA				0.3	V
		I_{out} = -1 mA				0.7	V
VIH_{M_DRV}	Logic High Threshold DELAY/M_DRV pin			1.5			V

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) The supply current excludes load and pull-up resistor current. Input pins are at GND or VDD.
(5) The accuracy for time interval settings below 1second is ±100ms.
(6) This parameter is specified by design and/or characterization and is not tested in production.
(7) Operational life time test procedure equivalent to10 years.

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6.6 Timing Requirements

			MIN(1)	NOM(2)	MAX(1)	UNIT
tr_{DRVn}	Rise Time DRVn(3)	Capacitive load 50 pF		50		ns
tf_{DRVn}	Fall Time DRVn(3)	Capacitive load 50 pF		50		ns
tD_{DONE}	DONE to DRVn delay	Min delay(4)		100		ns
		Max delay (4)		t_{DRVn}		
t_{M_DRV}	Valid manual MOSFET Power ON	Observation time 30ms	20			ms
t_{DB}	De-bounce manual MOSFET Power ON			20		ms

(1) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(3) This parameter is specified by design and/or characterization and is not tested in production.
(4) from DRVn rising edge.

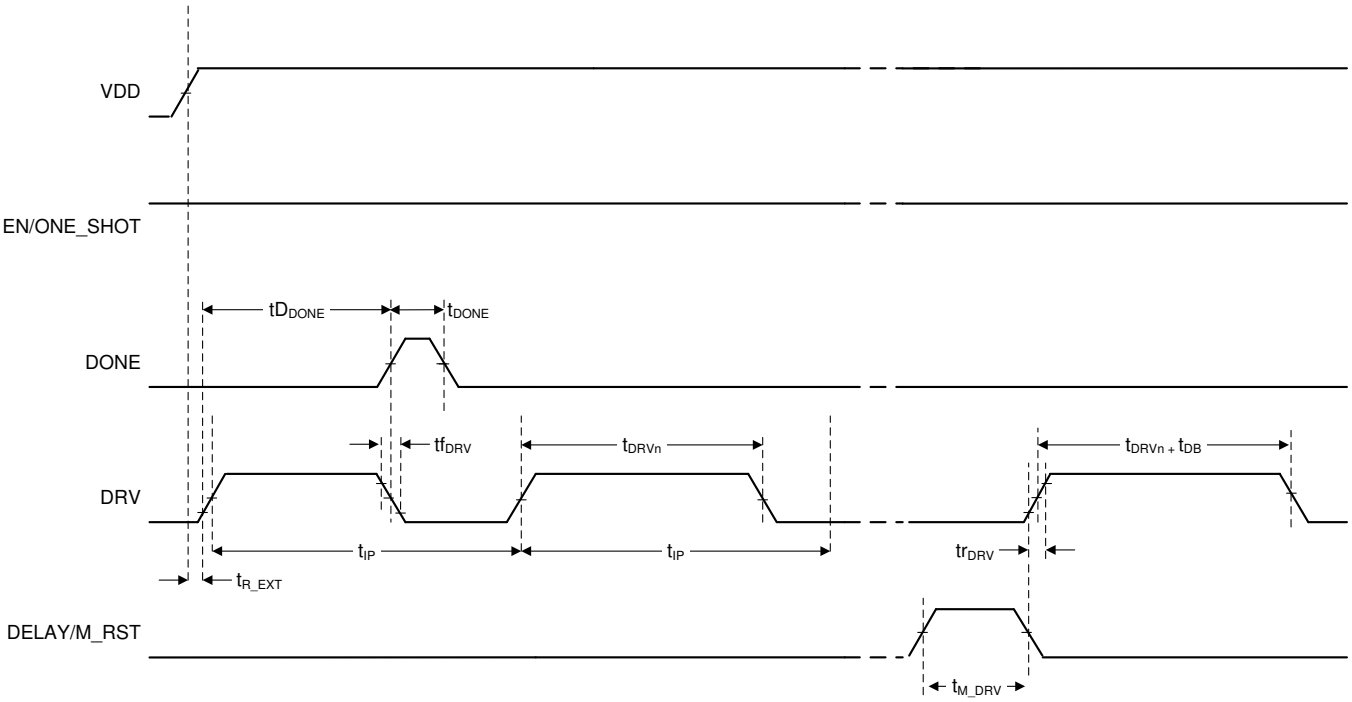


Figure 1. TPL5111 Timing

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6.7 Typical Characteristics

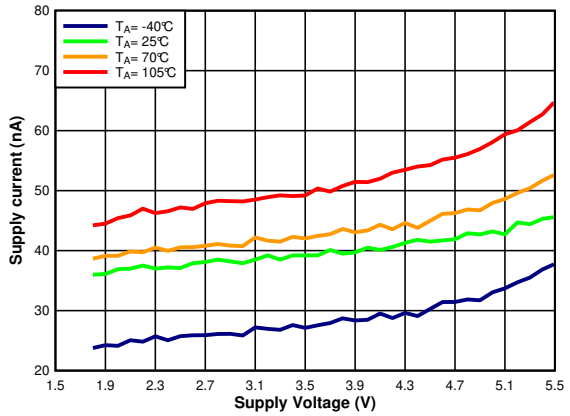


Figure 2. I_{DD} vs. V_{DD}

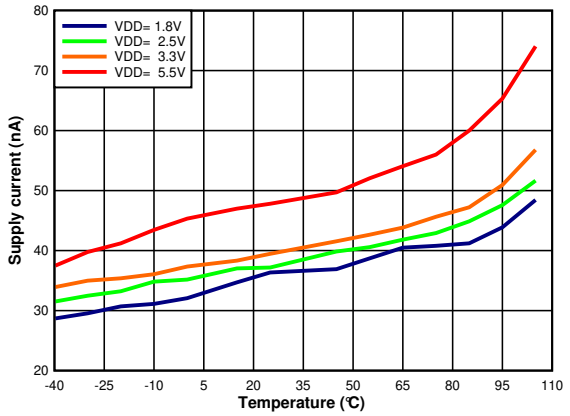


Figure 3. I_{DD} vs. Temperature

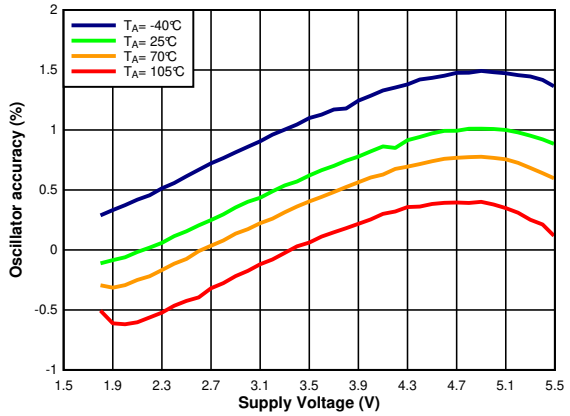


Figure 4. Oscillator Accuracy vs. V_{DD}

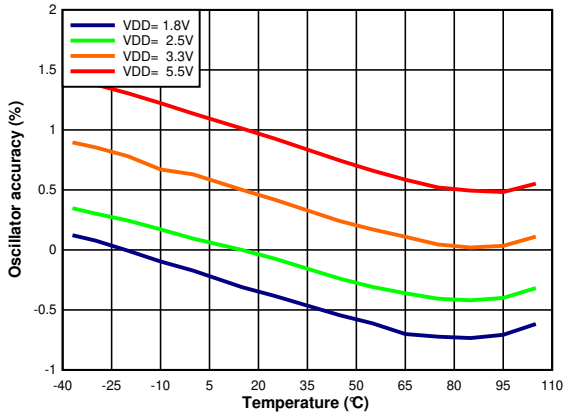


Figure 5. Oscillator Accuracy vs. Temperature

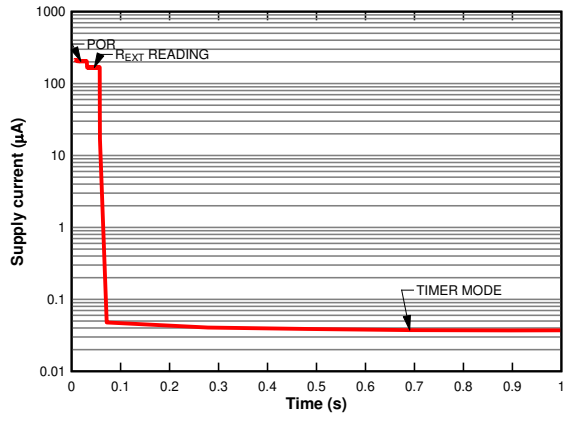


Figure 6. I_{DD} vs. Time

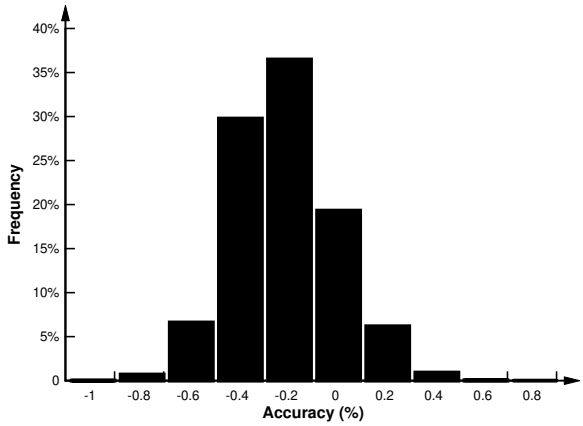


Figure 7. Time Interval Setting Accuracy

7 Detailed Description

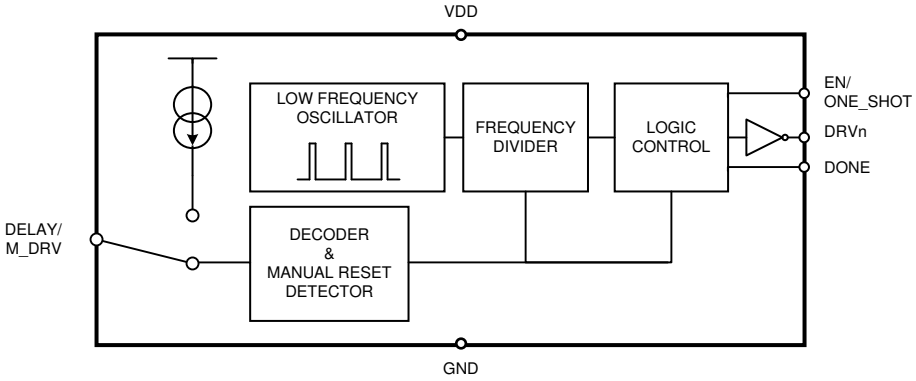
7.1 Overview

The TPL5111 is a timer with power gating feature. It is ideal for use in power-cycled applications and provides selectable timing from 100 ms to 7200 s.

When configured in timer mode (EN/ONE_SHOT= HIGH) the TPL5111 periodically asserts a DRVn signal to an LDO or DC-DC converter that is used to turn on a microcontroller. If the microcontroller replies with a DONE signal within the programmed time interval (< t_{DRVn}) the TPL5111 de-asserts DRVn. Otherwise the TPL5111 asserts DRVn for a time equal to t_{DRVn}.

The TPL5111 can also work in a one shot mode (EN/ONE_SHOT= LOW). In this mode the DRVn signal is asserted just one time at the power on of the TPL5111. If the µC replies with a DONE signal within the programmed time interval (< t_{DRVn}) the TPL5111 de-asserts DRVn. Otherwise the TPL5111 asserts DRVn for a time equal to t_{DRVn}.

7.2 Functional Block Diagram



7.3 Feature Description

The TPL5111 implements a periodic power gating feature or one shot power gating according to the EN/ONE_SHOT voltage. A manual Power ON function is realized by momentarily pulling the DELAY/M_DRV pin to VDD.

7.3.1 DRVn

The DRVn pin may be connected to the enable input of an LDO or DC-DC converter. The pulse generated at DRVn is equal to the programmed time interval period (t_{IP}), minus 50 ms. It is shorter if a DONE signal is received from the µC before t_{IP} - 50 ms. If the DONE signal is not received within t_{IP} - 50 ms, the DRVn signal will be LOW for the last 50 ms of t_{IP} before the next cycle starts.

The default value (after resistance reading) is HIGH. The signal is sent out from the TPL5111 when the programmed time interval starts. When the DRVn is HIGH, the manual power ON signal is ignored.

7.3.2 DONE

The DONE pin is driven by a µC to signal that the µC is working properly. The TPL5111 recognizes a valid DONE signal as a low to high transition; if two or more DONE signals are received within the time interval, only the first DONE signal is processed. The minimum DONE signal pulse length is 100 ns. When the TPL5111 receives the DONE signal it asserts DRVn logic LOW.

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7.4 Device Functional Modes

7.4.1 Startup

During startup, after POR, the TPL5111 executes a one-time measurement of the resistance attached to the DELAY/M_DRV pin in order to determine the desired time interval for DRVn. This measurement interval is t_{R_EXT}. During this measurement a constant current is temporarily flowing into R_{EXT}.

Once the reading of the external resistance is completed the TPL5111 enters automatically in one of the 2 modes according to the EN/ONE_SHOT value. The EN/ONE_SHOT pin must be hard wired to GND or VDD according to the required mode of operation.

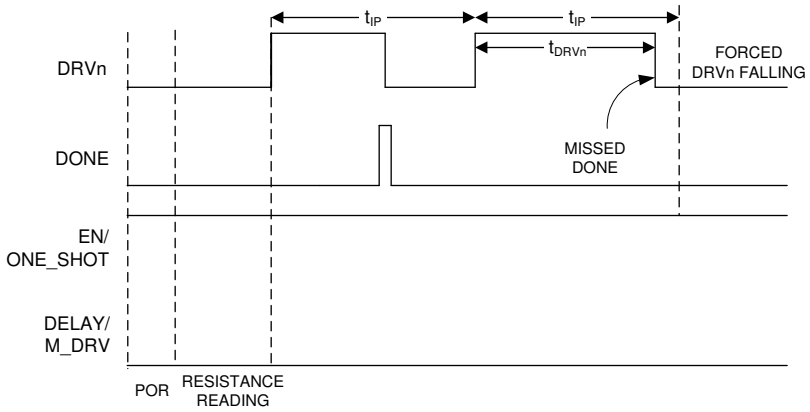


Figure 8. Startup - Timer Mode

7.4.2 Timer Mode

During timer mode (EN/ONE_SHOT = HIGH), the TPL5111 asserts periodic DRVn pulses according to the programmed time interval. The length of the DRVn pulses is set by the receiving of a DONE pulse from the uC. See Figure 8.

7.4.3 One Shot Mode

During One shot mode (EN/ONE_SHOT = LOW), the TPL5111 generates just one pulse at the DRVn pin which lasts according to the programmed time interval. In one-shot mode, other DRVn pulses can be triggered using the DELAY/M_DRV pin. If a valid manual power ON occurs when EN/ONE_SHOT is LOW, the TPL5111 generates just one pulse at the DRVn pin. The duration of the pulse is set by the programmed time interval. Also in this case, if a DONE signal is received within the programmed time interval (minus 50 ms), the DRVn output is asserted LOW. See Figure 9 and Figure 10.

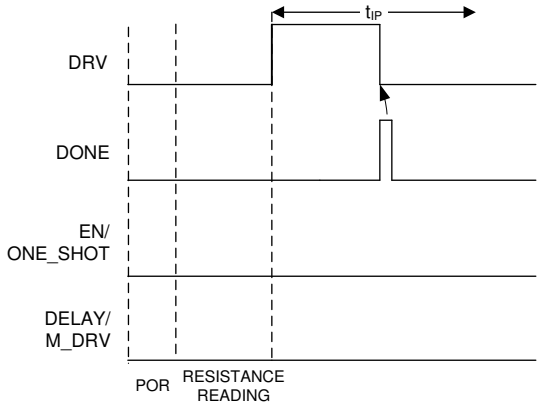


Figure 9. Startup One Shot Mode, (DONE Received within t_{IP})

Device Functional Modes (continued)

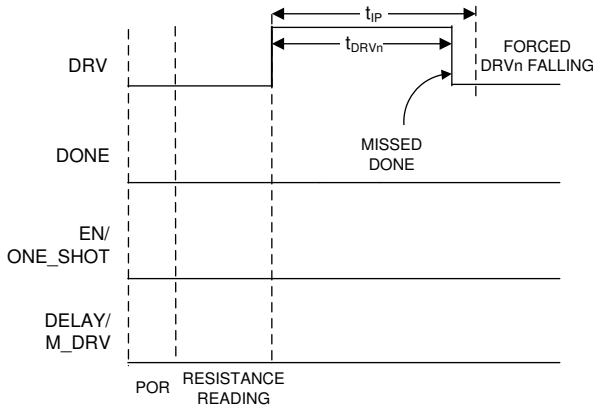


Figure 10. Startup One Shot Mode, (No DONE Received within t_{IP})

7.5 Programming

7.5.1 Configuring the Time Interval with the DELAY/M_DRV Pin

The time interval between 2 adjacent DRVn pulses (rising edges, in timer mode) is selectable through an external resistance (R_{EXT}) between the DELAY/M_DRV pin and ground. The resistance (R_{EXT}) must be in the range between 500 Ω and 170 kΩ. At least a 1% precision resistance is recommended. See *Selection of the External Resistance* on how to set the time interval using R_{EXT}. During startup, the external resistance is read immediately after POR.

7.5.2 Manual Power ON Applied to the DELAY/M_DRV Pin

If VDD is applied to the DELAY/M_DRV pin after startup is completed, the TPL5111 recognizes this as a manual Power ON condition. In this case R_{EXT} is not re-read. If the manual Power ON is asserted during the POR or during the R_{EXT} reading procedure, the reading procedure is aborted and is re-started as soon as the manual Power ON switch is released. A pulse on the DELAY/M_DRV pin is recognized as a valid manual Power ON only if it lasts at least 20ms (observation time is 30ms). If DRVn is already HIGH the manual Power ON is ignored. The manual Power ON may be implemented using a switch (momentary mechanical action).

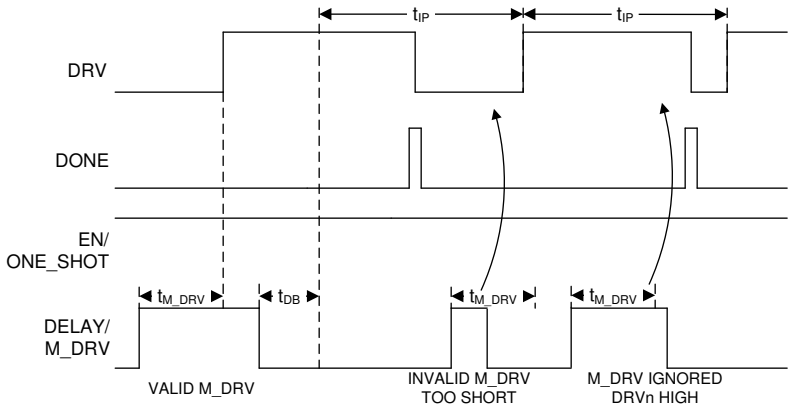


Figure 11. Manual Power ON in Timer Mode

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Programming (continued)

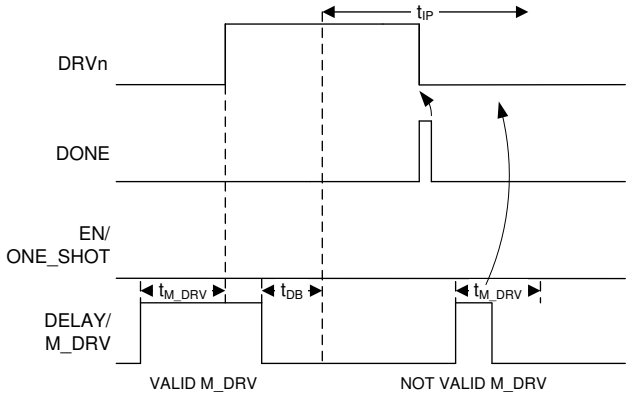


Figure 12. Manual Power ON in One Shot Mode

7.5.2.1 DELAY/M_DRV

A resistance in the range between 500Ω and 170kΩ must to be connected to the DELAY/M_DRV pin in order to select a valid time interval. At POR and during the reading of R_{EXT}, the DELAY/M_DRV pin is internally connected to an analog signal chain through a multiplexer. After the reading of R_{EXT}, the analog circuit is switched off and the DELAY/M_DRV pin is internally connected to a digital circuit.

In this state, a logic HIGH applied to the DELAY/M_DRV pin is interpreted by the TPL5111 as a manual power ON. The manual power ON detection is provided with a de-bounce feature (on both edges) which makes the TPL5111 insensitive to the glitches on the DELAY/M_DRV.

The DELAY/M_DRV pin must stay HIGH for at least 20ms to be valid. Once a valid signal at DELAY/M_DRV is understood as a manual power on, the DRVn signal will be asserted within the next 10ms. Its duration will be according to the programmed time interval (minus 50 ms), or less if the DONE is received.

A manual power ON signal resets all the counters. The counters will restart as soon as a valid manual power ON signal is recognized and the signal at DELAY/M_DRV pin is asserted LOW. Due to the asynchronous nature of the manual power ON signal and its arbitrary duration, the HIGH status of the DRVn signal may have an uncertainty of about ±5ms.

An extended assertion of a logic HIGH at the DELAY/M_DRV pin will turn on DRVn for a time longer than the programmed time interval. DONE signals received while the DELAY/M_DRV is HIGH are ignored. If the DRVn is already HIGH the manual power ON is ignored.

7.5.2.2 Circuitry

The manual Power ON may be implemented using a switch (momentary mechanical action). Using a single pole single throw (SPST) switch offers a low cost solution. The DELAY/M_DRV pin may be directly connected to V_{DD} with R_{EXT} in the circuit. The current drawn from the supply voltage during the manual power ON is given by V_{DD}/R_{EXT}.

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Programming (continued)

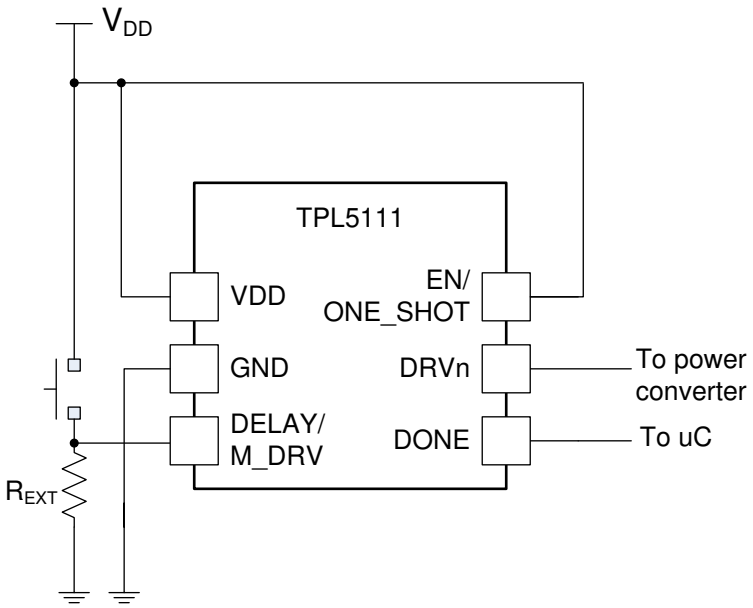


Figure 13. Manual Power ON with SPST Switch

7.5.3 Selection of the External Resistance

In order to set the time interval, the external resistance R_{EXT} is selected according the following formula:

$$R_{EXT} = 100 \left(\frac{-b + \sqrt{b^2 - 4a(c - 100\,T)}}{2a} \right) \quad (1)$$

Where:

- **T** is the desired time interval (t_{IP}) in seconds.
- $\mathbf{R_{EXT}}$ is the resistance value in Ω.
- **a**,**b**,**c** are coefficients depending on the value of the desired time interval. The coefficients are selected from Table 1 based on the range in which the desired t_{IP} falls.

Table 1. Coefficients for Equation 1

SET	TIME INTERVAL RANGE (S)	a	b	c
1	1 < T ≤ 5	0.2253	-20.7654	570.5679
2	5 < T ≤ 10	-0.1284	46.9861	-2651.8889
3	10 < T ≤ 100	0.1972	-19.3450	692.1201
4	100 < T ≤ 1000	0.2617	-56.2407	5957.7934
5	T > 1000	0.3177	-136.2571	34522.4680

EXAMPLE

Required time interval: 8s

Coefficient set number 2 is used in this case. The formula becomes

$$R_{EXT} = 100 \left(\frac{46.9861 - \sqrt{46.9861^2 + 4*0.1284(-2561.8889 - 100*8)}}{2*0.1284} \right) \quad (2)$$

The resistance value is 10.18 kΩ.

The following look-up-tables contain example values of t_{IP} and their corresponding value of R_{EXT}.

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Table 2. First 9 Time Intervals

t_{IP} (ms)	RESISTANCE (Ω)	CLOSEST REAL VALUE (Ω)	PARALLEL of TWO 1% TOLERANCE RESISTORS, (kΩ)
100	500	500	1.0 // 1.0
200	1000	1000	-
300	1500	1500	2.43 // 3.92
400	2000	2000	-
500	2500	2500	4.42 // 5.76
600	3000	3000	5.36 // 6.81
700	3500	3500	4.75 // 13.5
800	4000	4000	6.19 // 11.3
900	4500	4501	6.19 // 16.5

Table 3. Most Common Time Intervals Between 1s to 2h

t_{IP}	CALCULATED RESISTANCE (kΩ)	CLOSEST REAL VALUE (kΩ)	PARALLEL of TWO 1% TOLERANCE RESISTORS,(kΩ)
1s	5.20	5.202	7.15 // 19.1
2s	6.79	6.788	12.4 // 15.0
3s	7.64	7.628	12.7// 19.1
4s	8.30	8.306	14.7 // 19.1
5s	8.85	8.852	16.5 // 19.1
6s	9.27	9.223	18.2 // 18.7
7s	9.71	9.673	19.1 // 19.6
8s	10.18	10.180	11.5 // 8.87
9s	10.68	10.68	17.8 // 26.7
10s	11.20	11.199	15.0 // 44.2
20s	14.41	14.405	16.9 // 97.6
30s	16.78	16.778	32.4 // 34.8
40s	18.75	18.748	22.6 // 110.0
50s	20.047	20.047	28.7 // 66.5
1min	22.02	22.021	40.2 // 48.7
2min	29.35	29.349	35.7 // 165.0
3min	34.73	34.729	63.4 // 76.8
4min	39.11	39.097	63.4 // 102.0
5min	42.90	42.887	54.9 // 196.0
6min	46.29	46.301	75.0 // 121.0
7min	49.38	49.392	97.6 // 100.0
8min	52.24	52.224	88.7 // 127.0
9min	54.92	54.902	86.6 // 150.0
10min	57.44	57.437	107.0 // 124.0
20min	77.57	77.579	140.0 // 174.0
30min	92.43	92.233	182.0 // 187.0
40min	104.67	104.625	130.0 // 536.00
50min	115.33	115.331	150.0 // 499.00
1h	124.91	124.856	221.0 // 287.00
1h30min	149.39	149.398	165.0 // 1580.0
2h	170.00	170.00	340.0 // 340.0

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7.5.4 Quantization Error

The TPL5111 can generate 1650 discrete timer intervals in the range of 100 ms to 7200s. The first 9 intervals are multiples of 100ms. The remaining 1641 intervals cover the range between 1s to 7200s. Because they are discrete intervals, there is a quantization error associated with each value.

The quantization error can be evaluated according to the following formula:

$$Err = 100\frac{(T_{DESIRED} - T_{ADC})}{T_{DESIRED}} \quad (3)$$

Where:

$$T_{ADC} = INT\left[\frac{1}{100}\left(a\frac{R_D^2}{100^2} + b\frac{R_D}{100} + c\right)\right] \quad (4)$$

$$R_D = INT\left[\frac{R_{EXT}}{100}\right] \quad (5)$$

R_{EXT} is the resistance calculated with Equation 1 and a,b,c are the coefficients of the equation listed in Table 1.

7.5.5 Error Due to Real External Resistance

R_{EXT} is a theoretical value and may not be available in standard commercial resistor values. It is possible to closely approach the theoretical R_{EXT} using two or more standard values in parallel. However, standard values are characterized by a certain tolerance. This tolerance will affect the accuracy of the time interval.

The accuracy can be evaluated using the following procedure:

1. Evaluate the min and max values of R_{EXT} (R_{EXT_MIN}, R_{EXT_MAX} with Equation 1 using the selected commercial resistance values and their tolerances.
2. Evaluate the time intervals ($T_{ADC_MIN}[R_{EXT_MIN}]$, $T_{ADC_MAX}[R_{EXT_MAX}]$) with Equation 4.
3. Find the errors using Equation 3 with T_{ADC_MIN}, T_{ADC_MAX}.

The results of the formula indicate the accuracy of the time interval.

The example below illustrates the procedure.

- Desired time interval , T_desired = 600s,
- Required R_{EXT}, from Equation 1, R_{EXT}= 57.44kΩ.

From Table 3 R_{EXT} can be built with a parallel combination of two commercial values with 1% tolerance: R1=107kΩ, R2=124kΩ. The uncertainty of the equivalent parallel resistance can be found using:

$$uR_{//} = R_{//}\sqrt{\left(\frac{u_{R1}}{R1}\right)^2 + \left(\frac{u_{R2}}{R2}\right)^2} \quad (6)$$

Where uRn (n=1,2) represent the uncertainty of a resistance,

$$u_{Rn} = Rn\frac{Tolerance}{\sqrt{3}} \quad (7)$$

The uncertainty of the parallel resistance is 0.82%, meaning the value of R_{EXT} may range between R_{EXT_MIN} = 56.96 kΩ and R_{EXT_MAX} = 57.90 kΩ.

Using these values of R_{EXT}, the digitized timer intervals calculated with Equation 4 are respectively T_{ADC_MIN} = 586.85 s and T_{ADC_MAX} = 611.3 s, giving an error range of -1.88% / +2.19%. The asymmetry of the error range is due to the quadratic transfer function of the resistance digitizer.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In battery-powered applications one design constraint is the need for low current consumption. The TPL5111 is suitable in applications where there is a need to monitor environmental conditions at a fixed time interval, but at a very low rate. In these applications a watchdog or other internal timer in a µC is often used to implement a wakeup function. Typically, the power consumption of these timers is not optimized. Using the TPL5111 to implement a periodic power gating of the µC or of the entire system can reduce current consumption to only tens of nA.

8.2 Typical Application

The TPL5111 can be used in environment sensor nodes such as humidity and temperature sensor node. The measured the humidity and temperature data may be transmitted to a host controller through a low power RF micro such as the CC2531. Since the temperature and the humidity in a home application do not change quickly, the measurement and the transmission of the data can be done at very low rate, such as every 30 seconds. Using the TPL5111 as a system timer it is possible to completely turn off the RF micro when not transmitting and extend the battery life, as shown in Figure 14. The TPL5111 will turn on the LDO when the programmed time interval elapses. The manual Power ON switch can also be used to override the periodic turn-on behavior and enable on-demand power on.

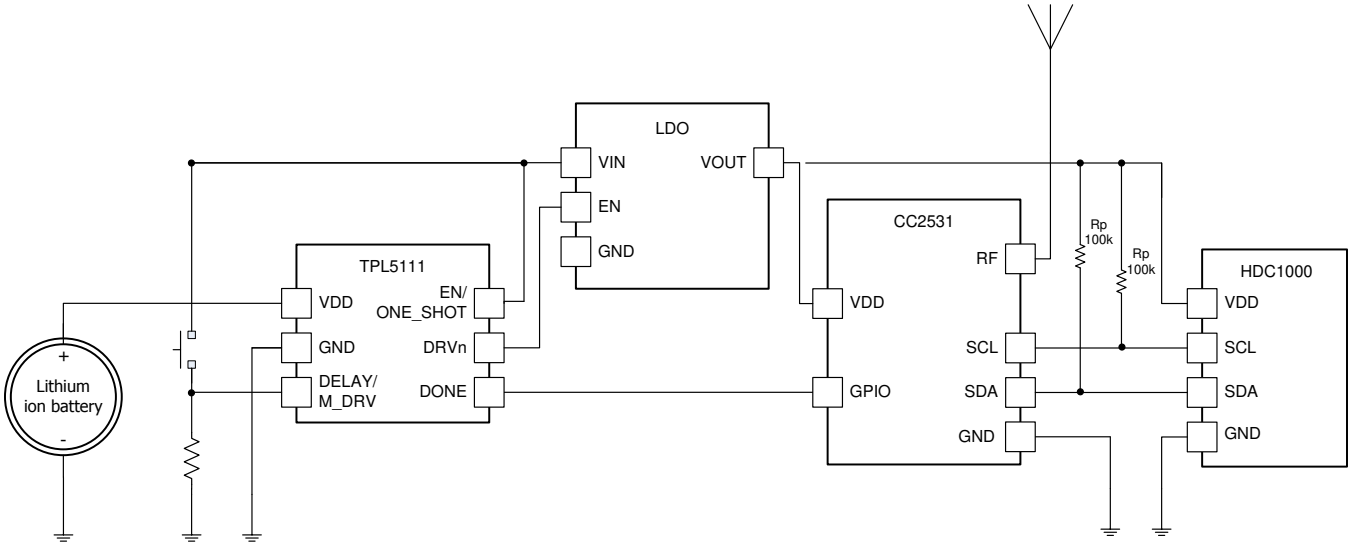


Figure 14. Sensor Node

8.2.1 Design Requirements

Assume that the system design requirements include a low current consumption constraint, in order to maximize battery life. The data may be acquired at a rate which is in the range between 30s and 60s, so the programmability of the TPL5111 allows optimization of system power consumption.

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Typical Application (continued)

8.2.2 Detailed Design Procedure

When the primary constraint is battery life, the selection of a low power voltage regulator or DC-DC converter to power the µC is mandatory. The first step in the design is to calculate the power consumption of each device in the different modes of operation. An example is the HDC1000 digital humidity and temperature sensor combined with an RF micro. In measurement mode the RF micro is in normal operating and transmission mode. The LDO or DC-DC converter should be selected to provide the necessary current source. For example, the HDC1000 consumes a maximum of 220 µA during a humidity measurement, and 300 µA during startup. The CC2531 consumes 29 mA in TX mode. The LDO should be capable of sourcing > 30 mA, which is an easy requirement to meet.

Assuming the desired wakeup interval is 30 seconds, then referring to Table 3, the values for parallel R_{EXT} resistors are 32.4 kΩ and 34.8 kΩ.

8.2.3 Application Curve

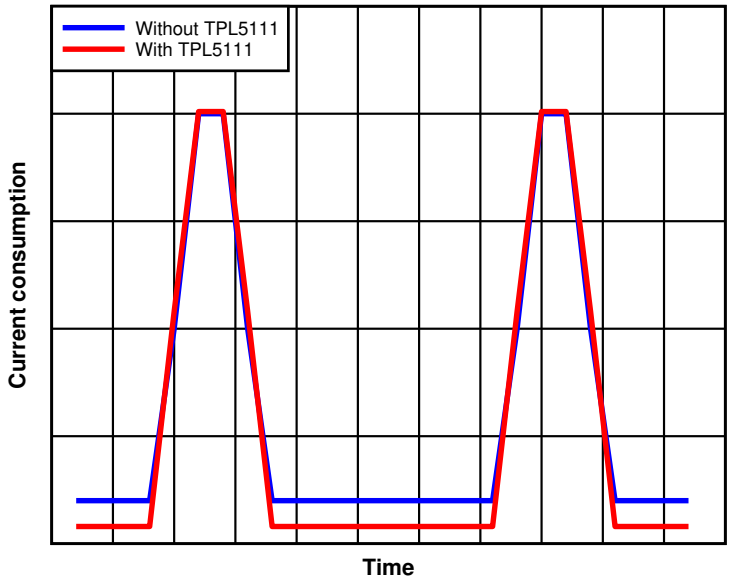


Figure 15. Effect of TPL5111 on Current Consumption

9 Power Supply Recommendations

The TPL5111 requires a voltage supply within 1.8 V and 5.5 V. A multilayer ceramic bypass X7R capacitor of 0.1 µF between VDD and GND pin is recommended.

10 Layout

10.1 Layout Guidelines

The DELAY/M_DRV pin is sensitive to parasitic capacitance. It is recommended that the traces connecting the resistance on this pin to GROUND be kept as short as possible to minimize parasitic capacitance. This capacitance can affect the initial set up of the time interval. Signal integrity on the DRVn pin is also improved by keeping the trace length between the TPL5111 and the enable input of the LDO/DC-DC converter short to reduce the parasitic capacitance. The EN/ONE_SHOT should to be tied to GND or VDD with short traces, and should never be left floating. The DONE input should never be left floating. If not tied to a µC GPIO, the DONE pin should be tied to ground.

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10.2 Layout Example

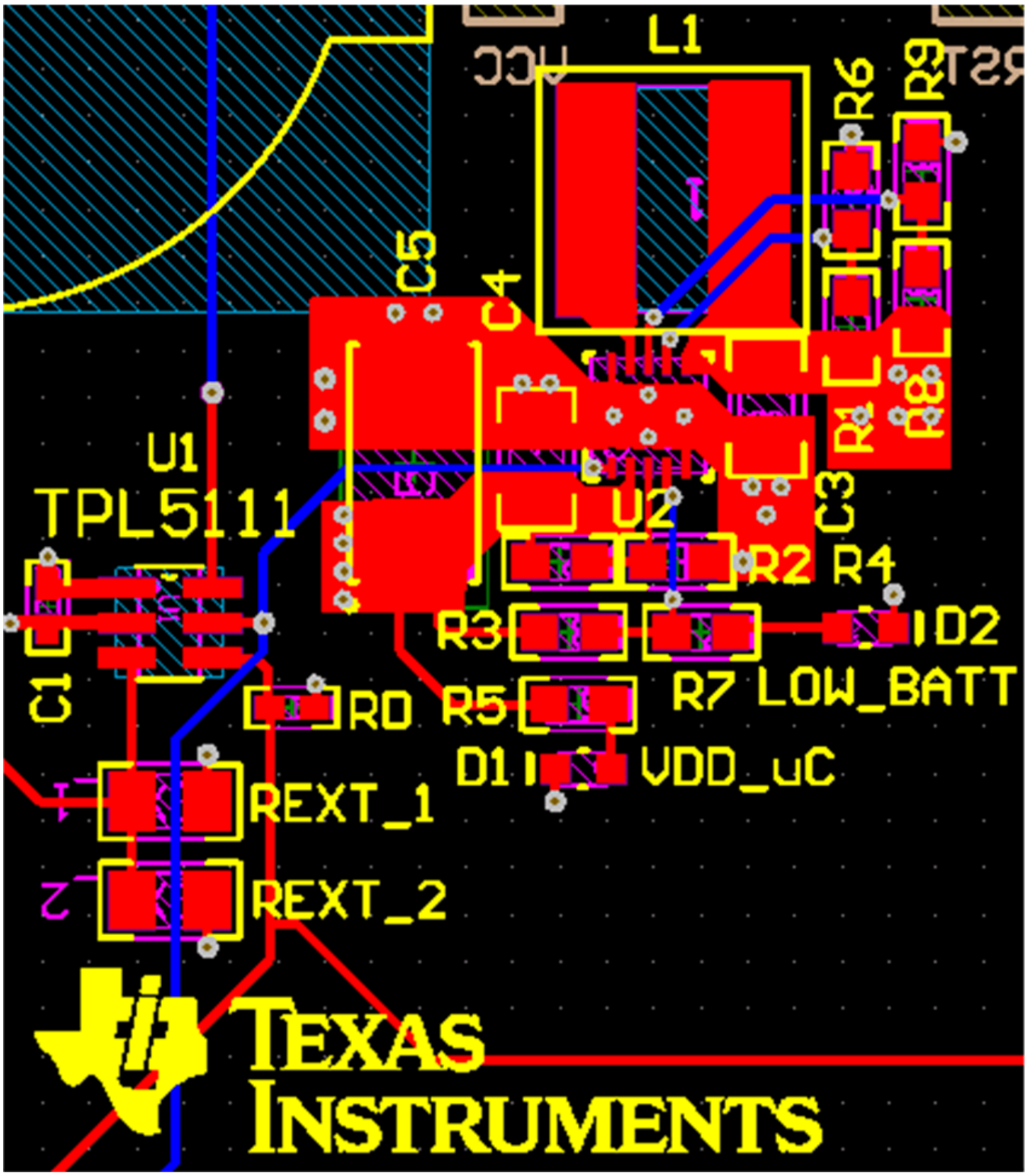


Figure 16. Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
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11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL5111DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZFVX	Samples
TPL5111DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZFVX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

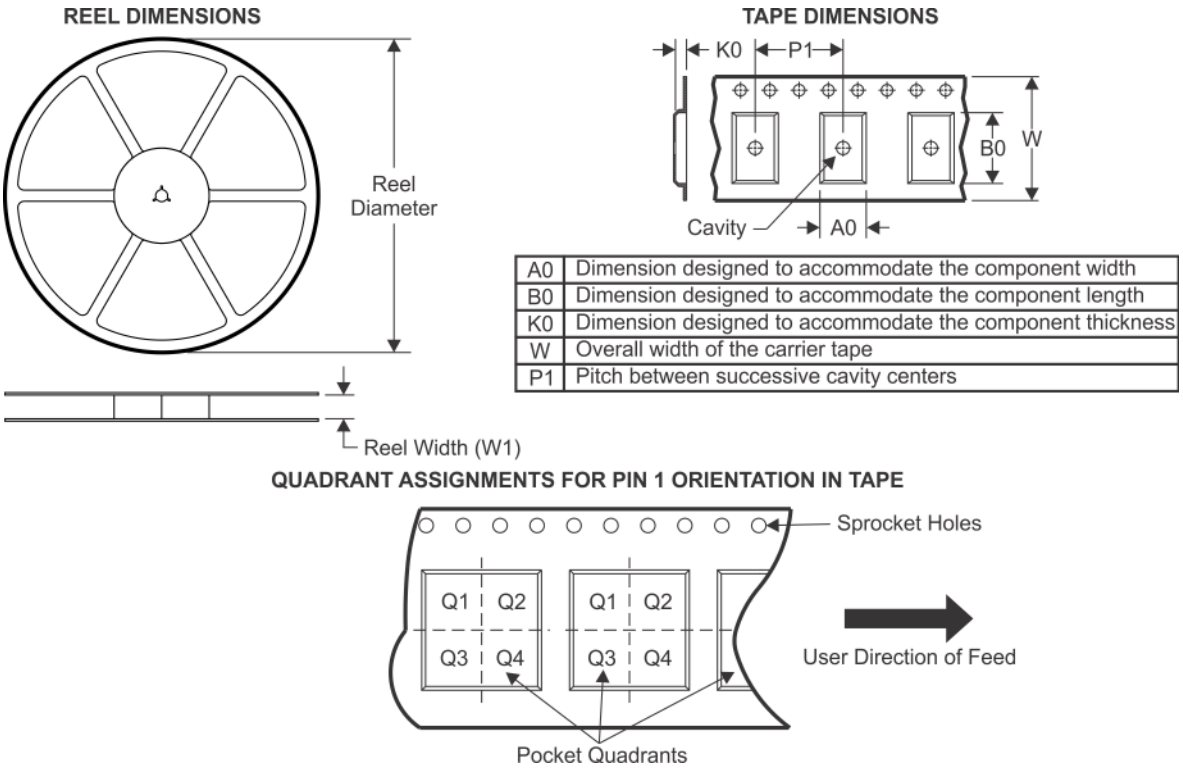
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

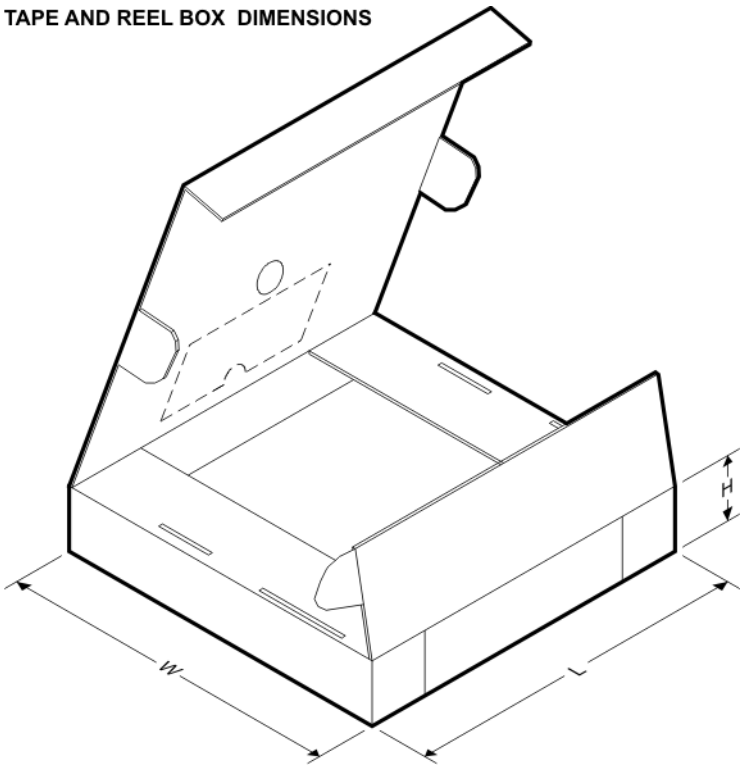


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL5111DDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPL5111DDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

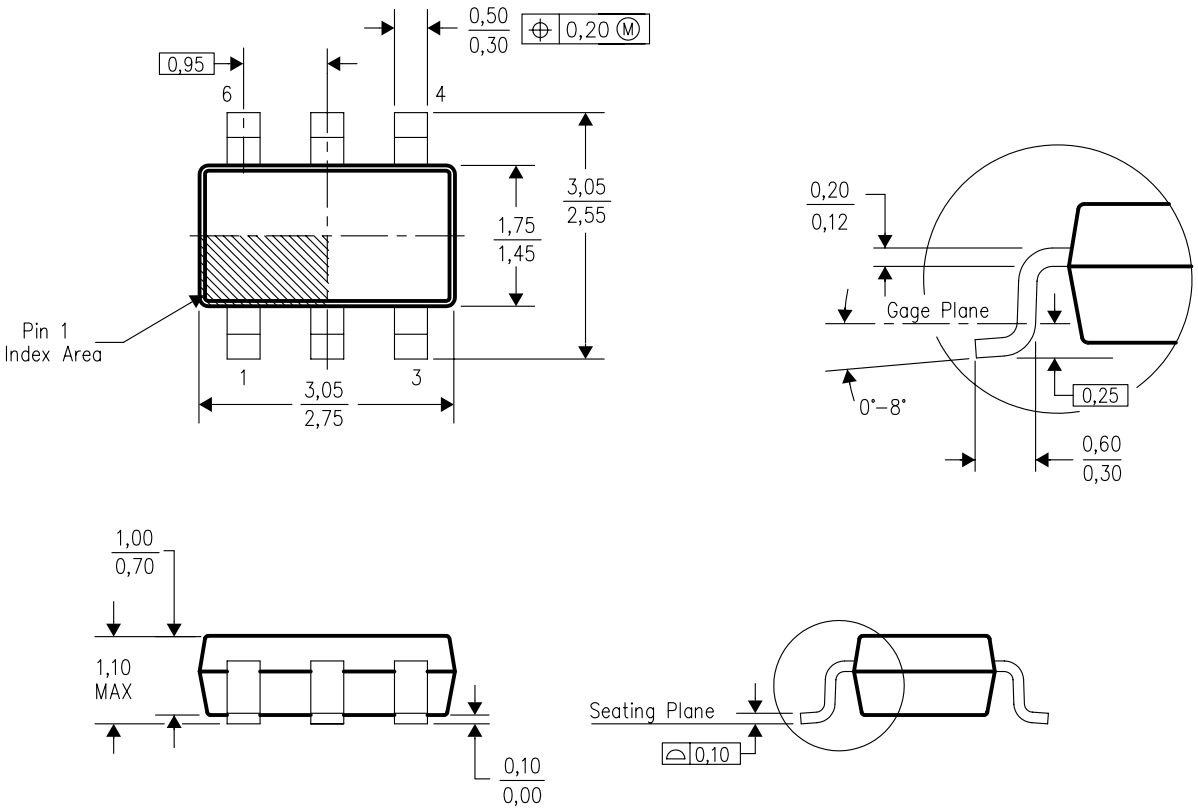
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL5111DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPL5111DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0

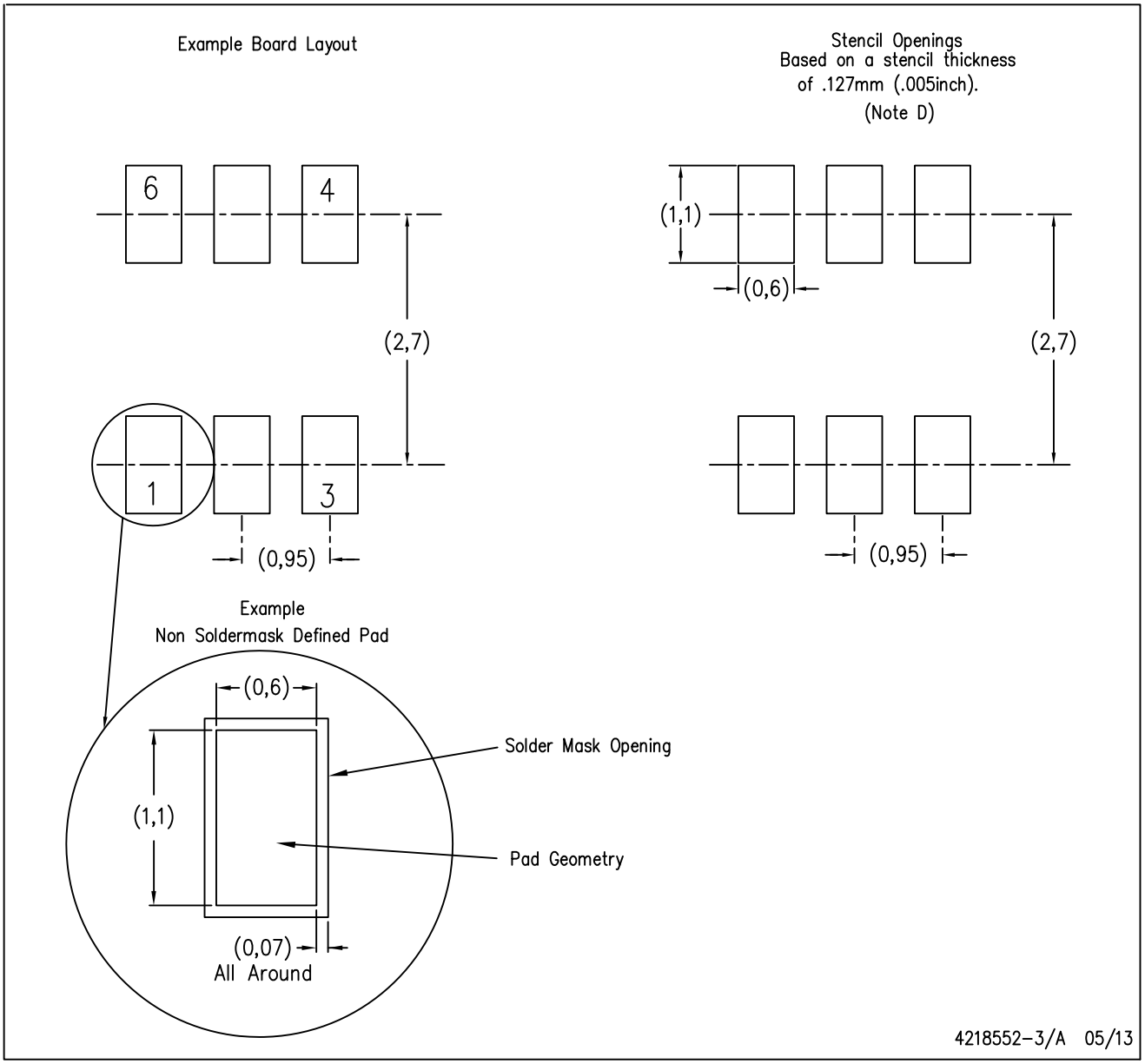
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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